

Advanced Analog Integrated Circuits

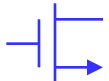
Basic Transistor Amplifiers

Bernhard E. Boser

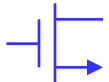
University of California, Berkeley

boser@eecs.berkeley.edu

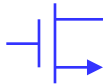
Copyright © 2016 by Bernhard Boser



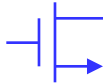
Design Example

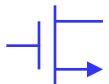


Topology

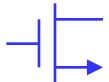


Small signal analysis

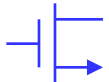




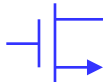
Dynamic Range



Dynamic Range



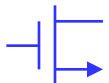
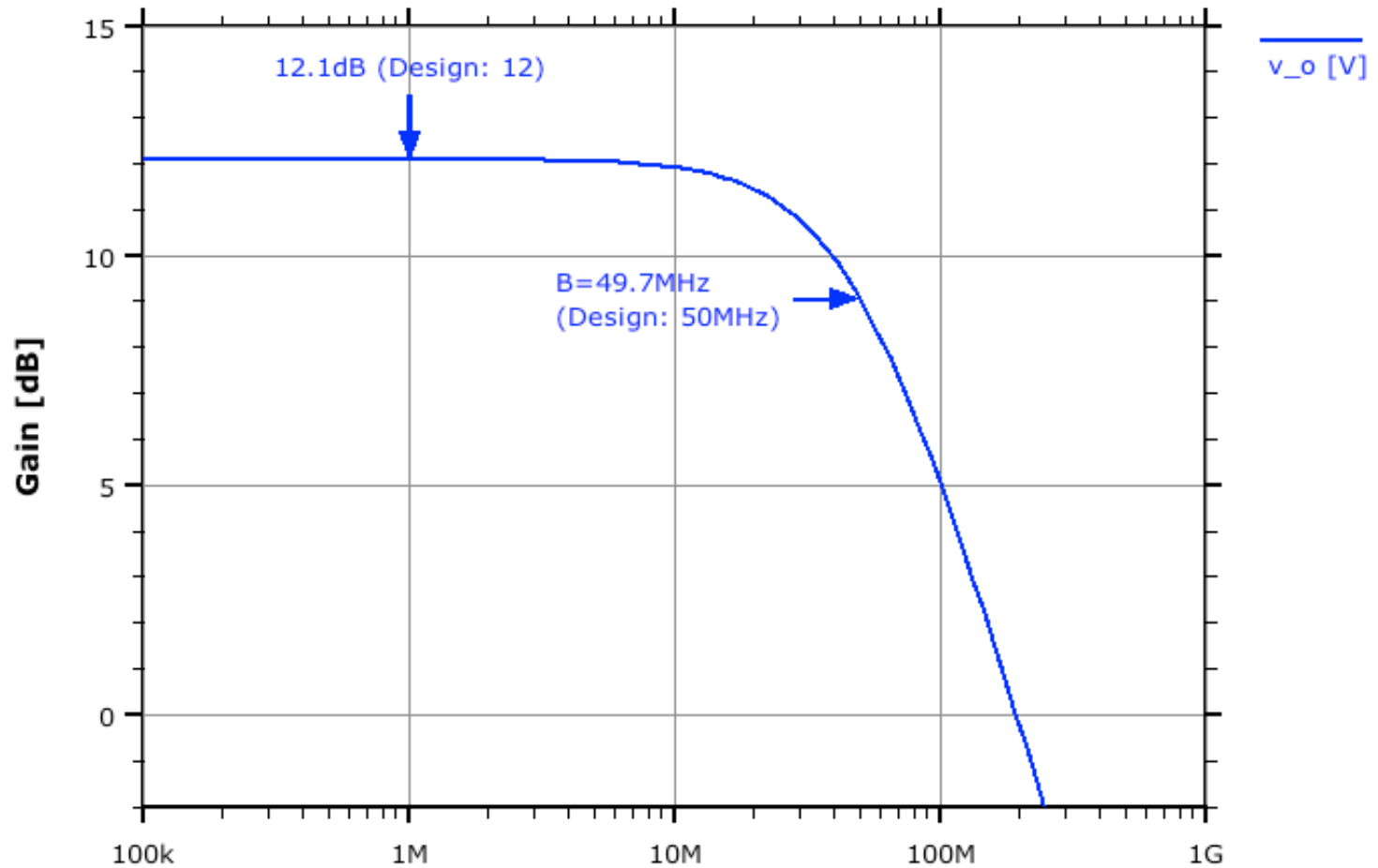
Solve



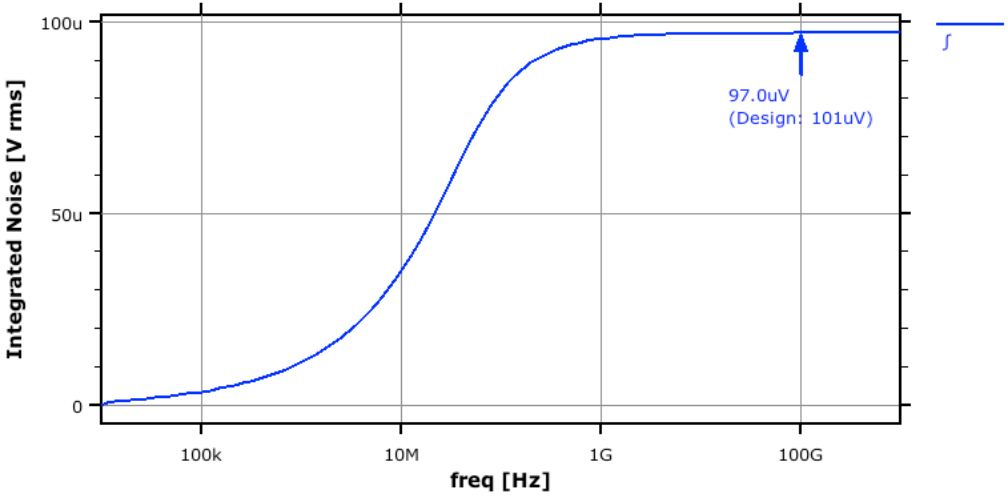
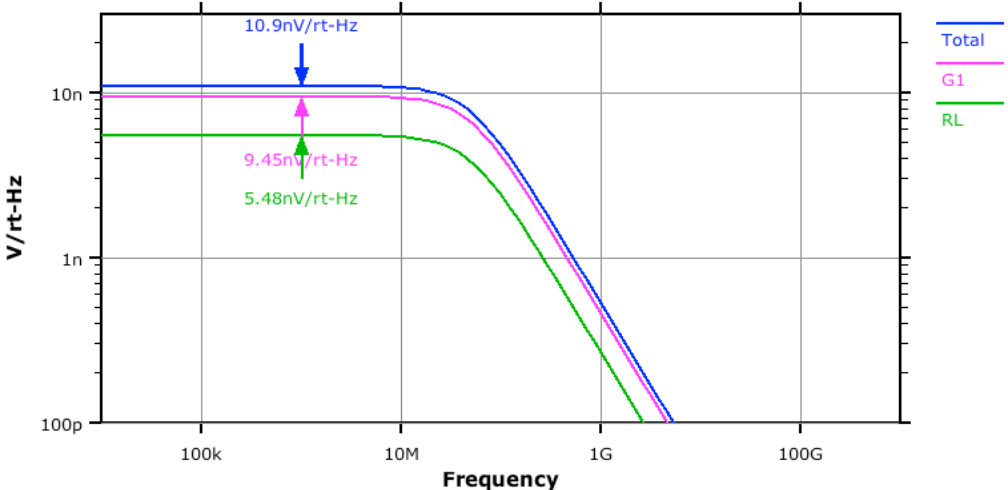
Verify



Gain and Bandwidth



Noise



What-If

Common Source

Specifications

Performance	$a_v := 4$	$B := 50\text{MHz}$	$\text{DR}_{\text{dB}} := 70 \text{ dB}$	$\text{DR} := 10^{\frac{\text{DR}_{\text{dB}}}{20}}$
Process	180nm CMOS	$V_{\text{DD}} := 1.8\text{V}$	$\gamma_n := 0.86$	

Design Equations

Low frequency gain

$$a_v = g_m \cdot R_L$$

3-dB Bandwidth

$$B = \frac{1}{2 \cdot \pi \cdot R_L \cdot C_L}$$

Dynamic Range

$$\text{DR} = \frac{\frac{1}{2} \cdot \left(\frac{r \cdot V_{\text{DD}}}{2}\right)^2}{\frac{k \cdot T}{C_L} \cdot (1 + \gamma_n \cdot a_v)}$$

Transistor specs:

$$L_1 := 180\text{nm} \quad V_{\text{star}} := 120\text{mV} \quad r := 0.5$$

Load capacitance

$$C_L := \text{DR} \cdot \frac{2 \cdot k_B \cdot T_f \cdot (1 + \gamma_n \cdot a_v)}{\left(r \cdot \frac{V_{\text{DD}}}{2}\right)^2} = 1.76 \cdot \text{pF}$$

Load resistance

$$R_L := \frac{1}{2 \cdot \pi \cdot B} \cdot \frac{1}{C_L} = 1.81 \cdot \text{k}\Omega$$

Transconductance

$$g_m := \frac{a_v}{R_L} = 2.21 \cdot \text{mS}$$

Bias current

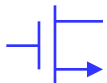
$$I_d := \frac{g_m \cdot V_{\text{star}}}{2} = 132 \cdot \mu\text{A} \quad R_L \cdot I_d = 240 \cdot \text{mV} \quad \frac{a_v \cdot V_{\text{star}}}{2} = 240 \cdot \text{mV}$$

Power dissipation

$$P_{\text{tot}} := V_{\text{DD}} \cdot I_d = 238 \cdot \mu\text{W} \quad \text{How can we reduce this?}$$

Total noise

$$v_{\text{oT}} := \sqrt{\frac{k_B \cdot T_f}{C_L} \cdot (1 + \gamma_n \cdot a_v)} = 101 \cdot \mu\text{V}$$



What-If: Reduce Power Dissipation?

Specifications

Performance	$a_v \approx 4$	$B \approx 50\text{MHz}$	$DR_{dB} \approx 70$ dB	$DR := 10^{\frac{DR_{dB}}{10}}$
Process	180nm CMOS	$V_{DD} \approx 1.8\text{V}$	$\gamma_n \approx 0.86$	

Design Equations

Low frequency gain

$$a_v = g_m \cdot R_L$$

3-dB Bandwidth

$$B = \frac{1}{2 \cdot \pi \cdot R_L \cdot C_L} \quad +$$

Dynamic Range

$$DR = \frac{\frac{1}{2} \cdot \left(\frac{r \cdot V_{DD}}{2} \right)^2}{\frac{k \cdot T}{C_L} \cdot (1 + \gamma_n \cdot a_v)}$$

Transistor specs:

$$L_1 \approx 180\text{nm} \quad V_{star} \approx 120\text{mV} \quad r \approx 0.5$$

Load capacitance

$$C_L \approx DR \cdot \frac{2 \cdot k_B \cdot T_r \cdot (1 + \gamma_n \cdot a_v)}{\left(r \cdot \frac{V_{DD}}{2} \right)^2} = 1.76 \cdot \text{pF}$$

Load resistance

$$R_L \approx \frac{1}{2 \cdot \pi \cdot B} \cdot \frac{1}{C_L} = 1.81 \cdot \text{k}\Omega$$

Transconductance

$$g_m \approx \frac{a_v}{R_L} = 2.21 \cdot \text{mS}$$

Bias current

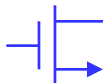
$$I_d \approx \frac{g_m \cdot V_{star}}{2} = 132 \cdot \mu\text{A} \quad R_L \cdot I_d = 240 \cdot \text{mV} \quad \frac{a_v \cdot V_{star}}{2} = 240 \cdot \text{mV}$$

Power dissipation

$$P_{tot} \approx V_{DD} \cdot I_d = 238 \cdot \mu\text{W} \quad \text{How can we reduce this?}$$

Total noise

$$v_{oT} \approx \sqrt{\frac{k_B \cdot T_r}{C_L} \cdot (1 + \gamma_n \cdot a_v)} = 101 \cdot \mu\text{V}$$



What-If: Reduced Power Dissipation

Specifications

Performance	$a_v := 4$	$B := 50\text{MHz}$	$DR_{\text{dB}} := 70$ dB	$DR := 10^{\frac{DR_{\text{dB}}}{10}}$
Process	180nm CMOS	$V_{\text{DD}} := 1.8\text{V}$	$\gamma_n := 0.86$	

Design Equations

Low frequency gain

$$a_v = g_m \cdot R_L$$

3-dB Bandwidth

$$B = \frac{1}{2 \cdot \pi \cdot R_L \cdot C_L} \quad +$$

Dynamic Range

$$DR = \frac{\frac{1}{2} \cdot \left(\frac{r \cdot V_{\text{DD}}}{2} \right)^2}{\frac{k \cdot T}{C_L} \cdot (1 + \gamma_n \cdot a_v)}$$

Transistor specs:

$$L_1 := 180\text{nm} \quad V_{\text{star}} := 120\text{mV} \quad r := 0.5$$

Load capacitance

$$C_L := DR \cdot \frac{2 \cdot k_B \cdot T_r \cdot (1 + \gamma_n \cdot a_v)}{\left(r \cdot \frac{V_{\text{DD}}}{2} \right)^2} = 1.76 \cdot \text{pF}$$

Load resistance

$$R_L := \frac{1}{2 \cdot \pi \cdot B} \cdot \frac{1}{C_L} = 1.81 \cdot \text{k}\Omega$$

Transconductance

$$g_m := \frac{a_v}{R_L} = 2.21 \cdot \text{mS}$$

Bias current

$$I_d := \frac{g_m \cdot V_{\text{star}}}{2} = 132 \cdot \mu\text{A} \quad R_L \cdot I_d = 240 \cdot \text{mV} \quad \frac{a_v \cdot V_{\text{star}}}{2} = 240 \cdot \text{mV}$$

Power dissipation

$$P_{\text{tot}} := V_{\text{DD}} \cdot I_d = 238 \cdot \mu\text{W} \quad \text{How can we reduce this?}$$

Total noise

$$v_{\text{oT}} := \sqrt{\frac{k_B \cdot T_r}{C_L} \cdot (1 + \gamma_n \cdot a_v)} = 101 \cdot \mu\text{V}$$

Specifications

Performance	$a_v := 4$	$B := 50\text{MHz}$	$DR_{\text{dB}} := 70$ dB	$DR := 10^{\frac{DR_{\text{dB}}}{10}}$
Process	180nm CMOS	$V_{\text{DD}} := 1.8\text{V}$	$\gamma_n := 0.86$	

Design Equations

Low frequency gain

$$a_v = g_m \cdot R_L$$

3-dB Bandwidth

$$B = \frac{1}{2 \cdot \pi \cdot R_L \cdot C_L}$$

Dynamic Range

$$DR = \frac{\frac{1}{2} \cdot \left(\frac{r \cdot V_{\text{DD}}}{2} \right)^2}{\frac{k \cdot T}{C_L} \cdot (1 + \gamma_n \cdot a_v)}$$

Transistor specs:

$$L_1 := 180\text{nm} \quad V_{\text{star}} := 120\text{mV} \quad r := 0.75$$

Load capacitance

$$C_L := DR \cdot \frac{2 \cdot k_B \cdot T_r \cdot (1 + \gamma_n \cdot a_v)}{\left(r \cdot \frac{V_{\text{DD}}}{2} \right)^2} = 0.78 \cdot \text{pF} \quad +$$

Load resistance

$$R_L := \frac{1}{2 \cdot \pi \cdot B} \cdot \frac{1}{C_L} = 4.08 \cdot \text{k}\Omega$$

Transconductance

$$g_m := \frac{a_v}{R_L} = 0.98 \cdot \text{mS}$$

Bias current

$$I_d := \frac{g_m \cdot V_{\text{star}}}{2} = 59 \cdot \mu\text{A} \quad R_L \cdot I_d = 240 \cdot \text{mV} \quad \frac{a_v \cdot V_{\text{star}}}{2} = 240 \cdot \text{mV}$$

Power dissipation

$$P_{\text{tot}} := V_{\text{DD}} \cdot I_d = 106 \cdot \mu\text{W} \quad \text{How can we reduce this?}$$

Total noise

$$v_{\text{oT}} := \sqrt{\frac{k_B \cdot T_r}{C_L} \cdot (1 + \gamma_n \cdot a_v)} = 151 \cdot \mu\text{V}$$



Advanced Analog Integrated Circuits

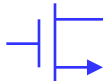
Check: Verification with “Real” Transistor

Bernhard E. Boser

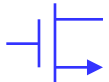
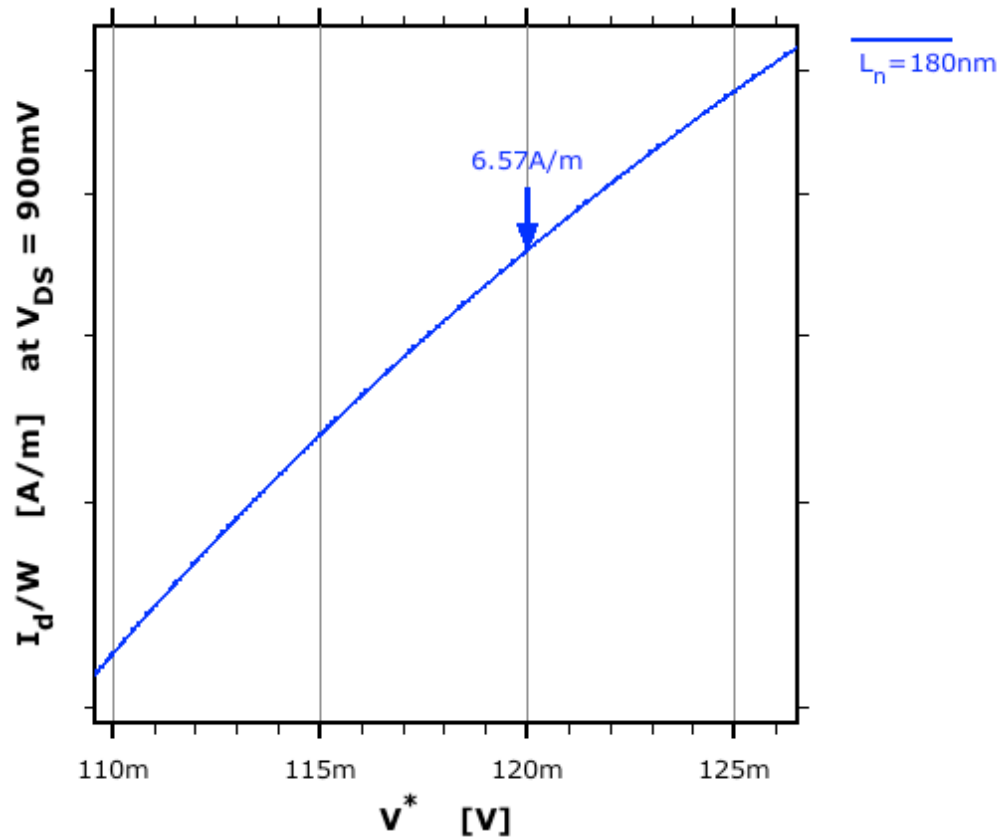
University of California, Berkeley

boser@eecs.berkeley.edu

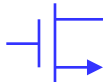
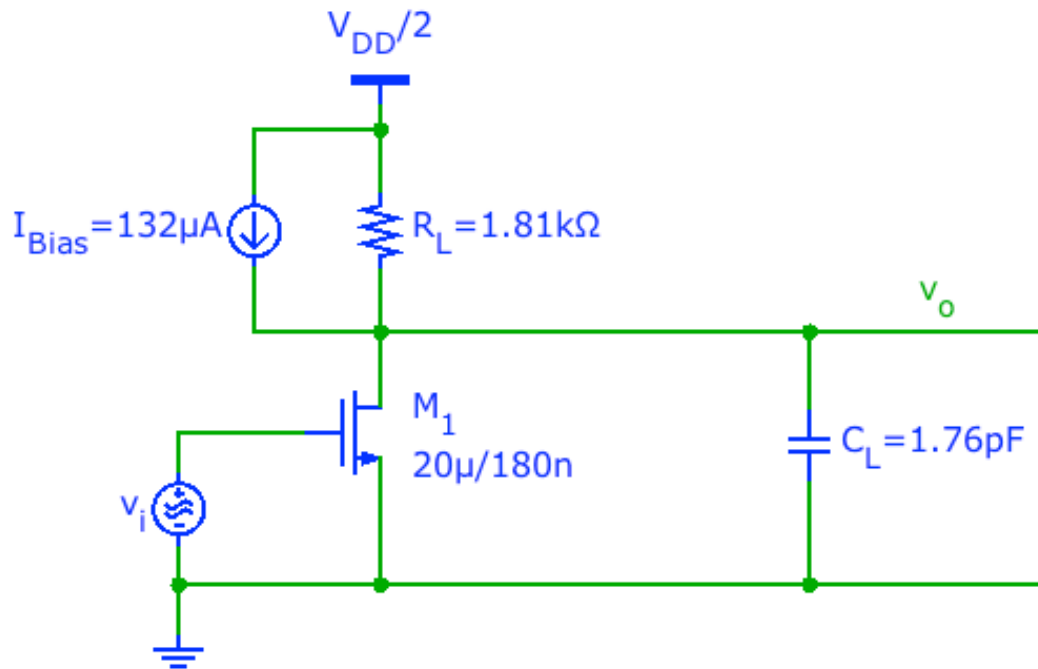
Copyright © 2016 by Bernhard Boser



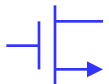
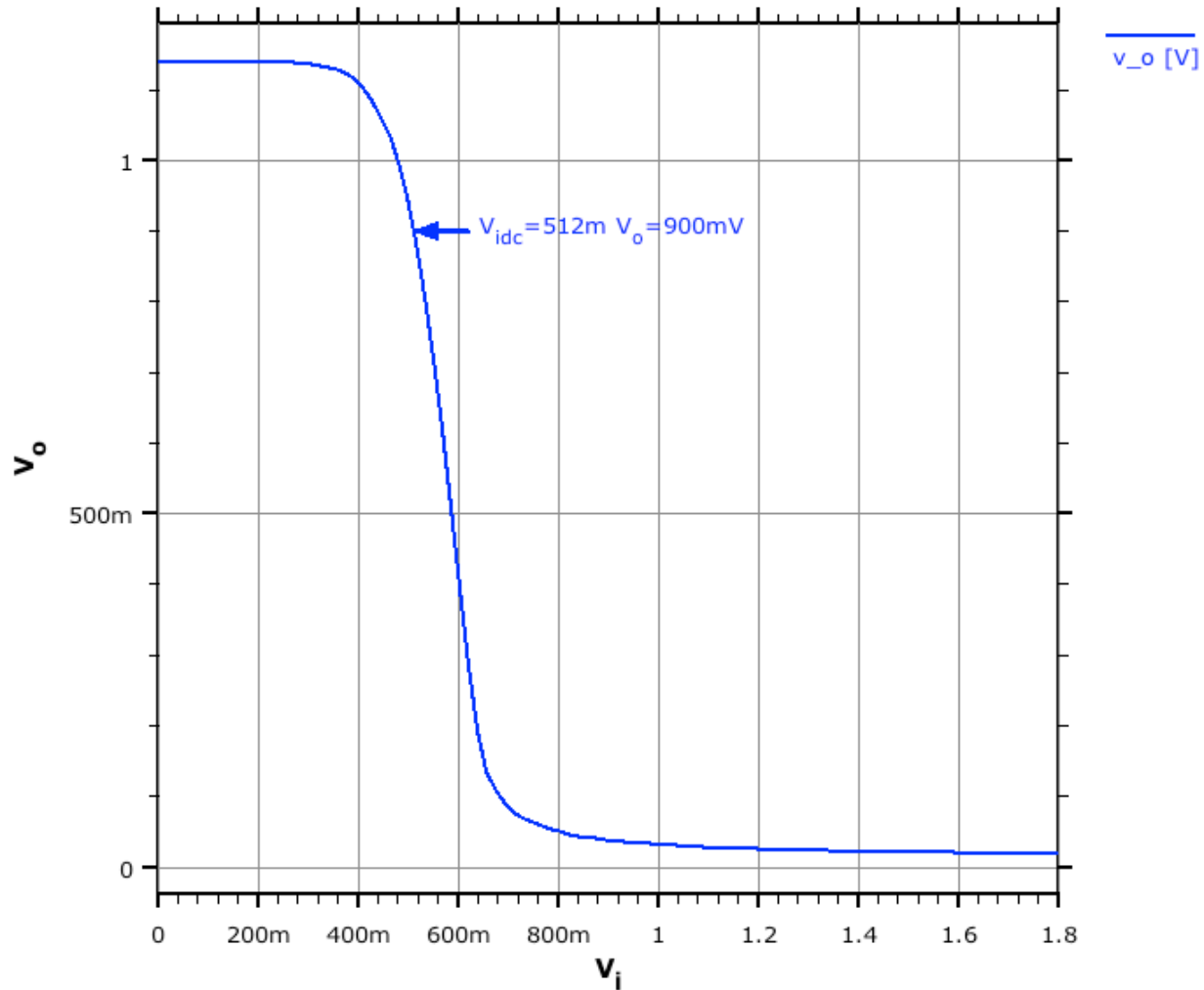
But ... what about a “real” transistor?



Biasing ...

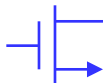


DC Operating Point

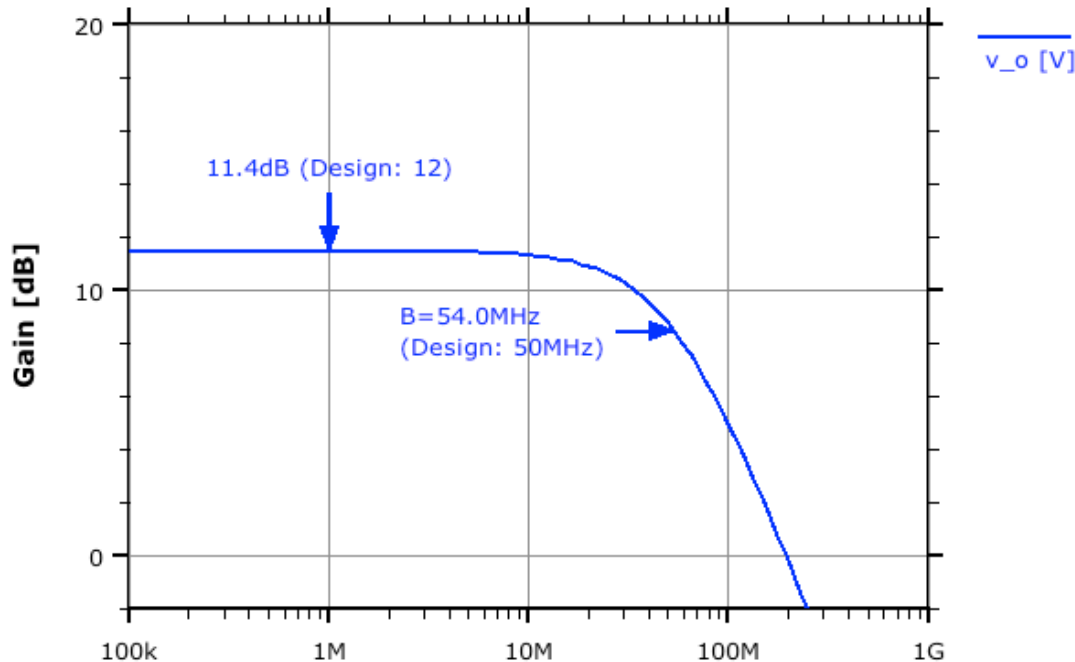


Transistor Operating Point Check

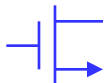
```
M1: bsim3v3
d : V(root.v_o) = 899.066 mV
g : V(root.vgs) = 512 mV
s : val(0) = 0
b : val(0) = 0
    type = n
    region = subth
    reversed = no
    ids = 132.516 uA 132uA
    isub = 42.2913 pA
    vgs = 512 mV
    vds = 899.066 mV 900mV
    vbs = 0 V
    vgb = 512 mV
    vdb = 899.066 mV
    vgd = -387.066 mV
    vth = 514.279 mV
    vdsat = 69.4368 mV
    vfbEFF = -1.09875 V
    gm = 2.24692 mS 2.21mS
    gds = 50.2374 uS
    gmbs = 644.535 uS
    betaEFF = 65.1953 mA/V^2
    cjd = 10.2586 fF
    cjs = 11.7154 fF
    qb = -18.5858 fCoul
    qg = 19.9153 fCoul
    qg = 19.9153 fCoul
    qd = 2.86107 fCoul
    qbd = -10.6792 fCoul
    qbs = -105.569e-21 Coul
    cgg = 29.5591 fF
    cgd = -7.34957 fF
    cgs = -15.5588 fF
    cgb = -6.65065 fF
    cdg = -7.39886 fF
    cdd = 17.6518 fF
    cds = 7.46008 aF
    cdb = -10.2604 fF
    csg = -15.9526 fF
    csd = -25.7075 aF
    css = 30.1804 fF
    csb = -14.2021 fF
    cbg = -6.20759 fF
    cbd = -10.2765 fF
    cbs = -14.629 fF
    cbb = 31.1131 fF
    ron = 6.78457 kOhm
    id = 132.516 uA
    is = -132.516 uA
    ibulk = -42.2919 pA
    ibs = -41.3032 aA
    ibd = -42.2919 pA
    pwr = 119.141 uW
    gmoverid = 16.9558 1/V 16.7 /V
    cgsov1 = 7.3926 fF
    cgdov1 = 7.3926 fF
    cgbov1 = 26.5891 aF
    i1 = 132.516 uA
    i3 = -132.516 uA
    i4 = -42.2919 pA
    gbd = 776.844 pS
    gbs = 4.58359 pS
    vgsteff = 36.6265 mV
    qinv = 2.08789 mCoul
    igd = 0 A
    igs = 0 A
    igb = 0 A
    qgi = 18.9781 fCoul
    qsi = -405.587 aCoul
    qdi = -289.142e-21 Coul
    qbi = -18.5722 fCoul
    cddb1 = 611.498e-21 F
    cssb1 = 11.0724 fF
    cggbi = 14.7473 fF
    cgsbi = -8.16625 fF
    cgdb1 = 43.0261 aF
    cbdb1 = -17.93 aF
    cbsbi = -2.91363 fF
    qsrco = -4.19053 fCoul
```



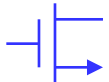
Gain and Bandwidth



- Gain below spec
- $11.4\text{dB} = 3.7 < 4$
- Why?
- Transistor a_{v_o}
 - From operating point analysis:
 $g_m/g_{ds} = 44.8$
 - $\sim 10\%$ error on gain of 4
- Note: only @ operating point, amplifier is quite nonlinear and the output range limited by R_L



Conclusions



Advanced Analog Integrated Circuits

Common Gate Stage

Bernhard E. Boser

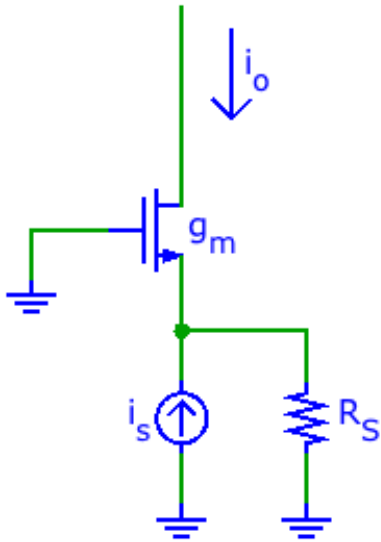
University of California, Berkeley

boser@eecs.berkeley.edu

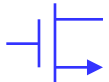
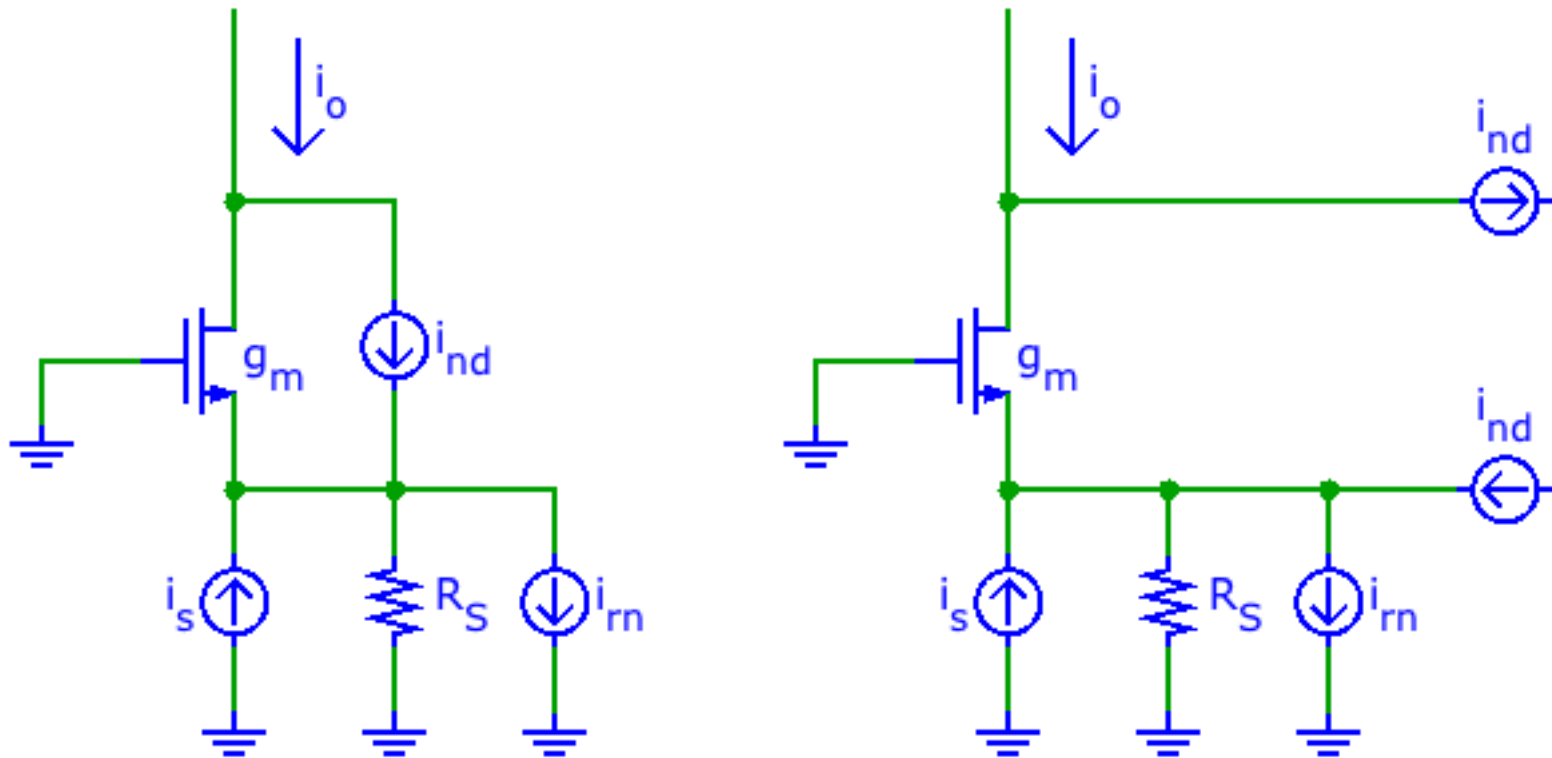
Copyright © 2016 by Bernhard Boser



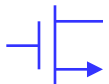
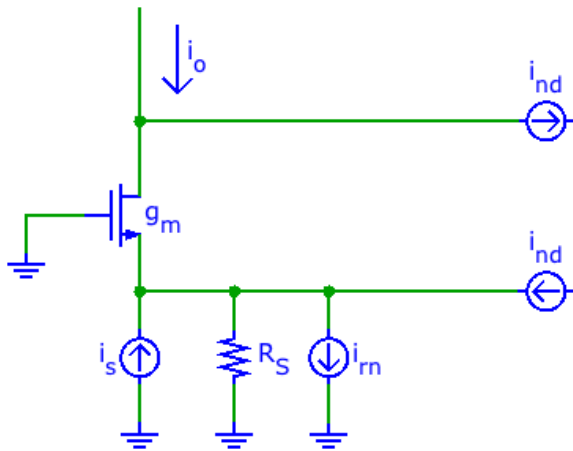
Common Gate Stage



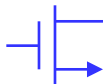
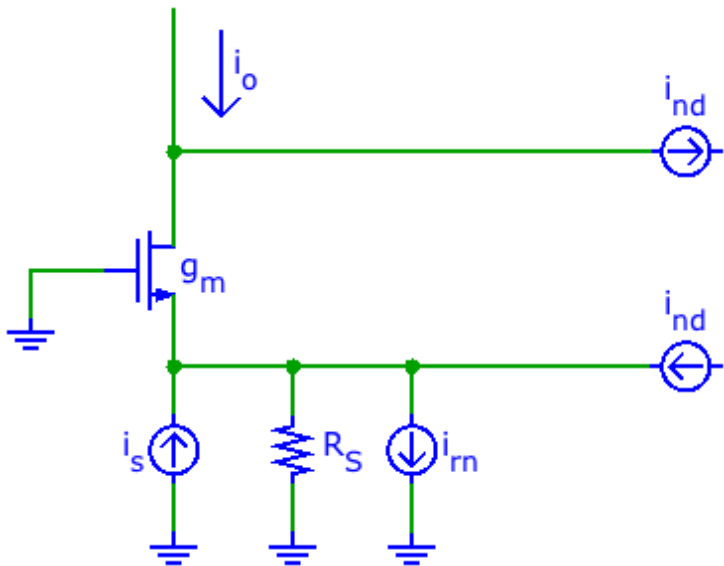
CG Noise Sources



CG Noise Analysis



CG Noise at High Frequency



Advanced Analog Integrated Circuits

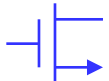
Source Follower

Bernhard E. Boser

University of California, Berkeley

boser@eecs.berkeley.edu

Copyright © 2016 by Bernhard Boser



Source Follower

